Application Note
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Silicon Carbide Power Modules

1. Introduction

This application note provides an introduction to silicon carbide (SiC) MOSFET devices in industrial power semiconductor modules. It is targeted towards users familiar with silicon (Si) power semiconductors (primarily IGBTs) and focuses on the power modules offered by Semikron Danfoss which presently include the devices with the following characteristics:

- n-type, enhancement-mode, MOSFETs
- planar or trench gate
- blocking voltage 650…1700V
- drain current >20A

The behavior of SiC Schottky Barrier Diodes (SBD) is covered separately in [3].

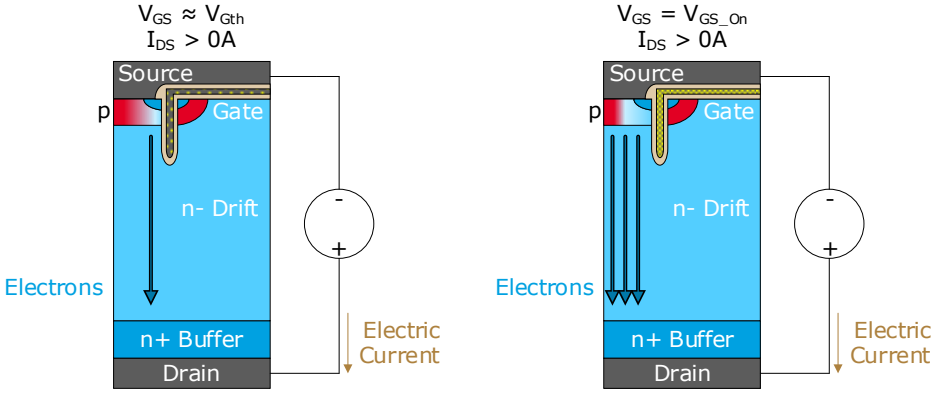
At the time of publication, SiC MOSFET technology is still rapidly developing so the information provided herein should be viewed in the context of a particular chip generation.

2. Static Behavior

2.1 Conducting state

The basic operation of a SiC MOSFET is the same as a Si device where the gate is used to control current flow between drain and source. When the gate is off ($V_{GS} \leq 0V$), the channel is closed and the device blocks. When the gate voltage rises above the threshold voltage ($V_{GS} > V_{GS(th)}$), the channel begins to open (p-region is inverted by the electric field and the pn junction vanishes locally) and current can flow. As the gate voltage is increased, more and more of the channel is opened (more of the p-region is inverted) resulting in a lower channel resistance and therefore a lower total $R_{DS(on)}$. The critical field strength of SiC is much higher than for Si, therefore can be the n- Drift region much thinner compared to Si and the forward voltage drop is much lower.

Figure 1: Partial (L) and full (R) forward conduction

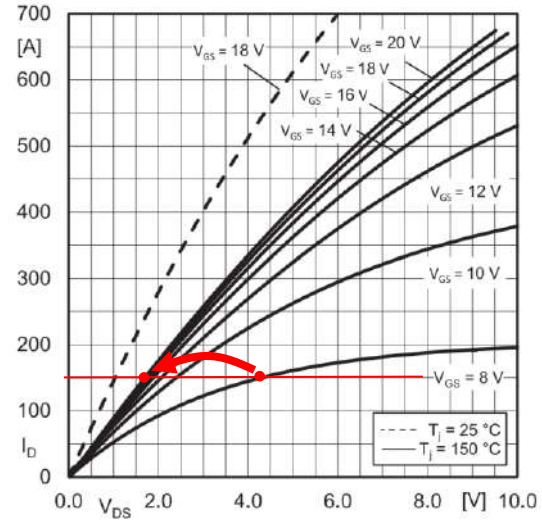


A higher gate voltage is often desirable to reduce conduction losses to a minimum. An increasing gate voltage gives a lower drain-source voltage for a given current (Figure 2). However, the lower losses must be balanced with other factors. A higher V_{GS} results in a more open channel, allowing a higher short circuit current to flow, and increases the stress during the pulse. Short circuit pulses must be detected quickly and turned off, or the MOSFET will be destroyed.

At high currents, $R_{DS(on)}$ becomes nonlinear. $R_{DS(on)}$ is a function of current and increases with rising current. For very high currents, the MOSFET goes in desaturation with an almost horizontal output characteristic as shown in Figure 2 for V_{GS} = 8V. The desaturation level increases with higher gate voltages and decreases with higher temperatures.

For example, the I_D vs. V_{DS} curve bends sharply with V_{GS} = 8V, as shown in Figure 2. However, at V_{GS} = 15V, this effect is much less visible. For the purposes of loss calculations, this effect is ignored and one $R_{DS(on)}$ value is provided for a given temperature. The nonlinear operating space is typically avoided, so there is relatively little error in using a single $R_{DS(on)}$ value, but the calculation is much simpler.

Figure 2: Influence of gate voltage on voltage drop (SKM350MB120SCH15)



The behavior of SiC MOSFETs changes with temperature, most notably the on-state resistance ($R_{DS(on)}$). The effect of this is seen in the voltage-current characteristics of the device in forward and reverse directions (Figure 3). $R_{DS(on)}$ has a strong positive temperature coefficient, meaning that as the temperature increases, $R_{DS(on)}$ also increases. This provides an inherent balancing between paralleled chips and modules.

Figure 3: MOSFET forward and reverse voltage drops vs. temperature (V_{GS} >> 0V)

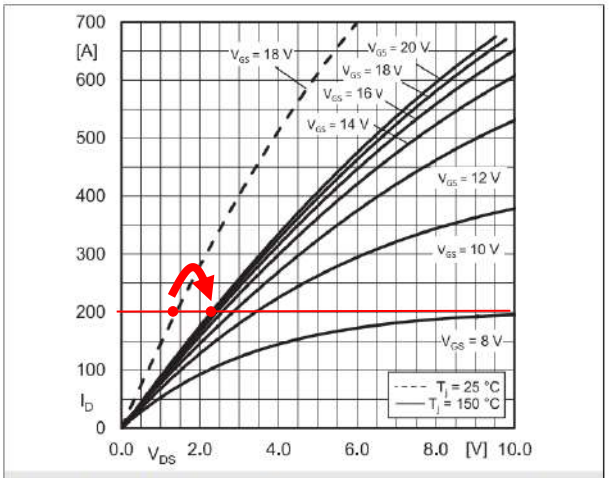


Fig.1: Typ. MOSFET forward output characteristic, incl. $R_{DD'+SS'}$

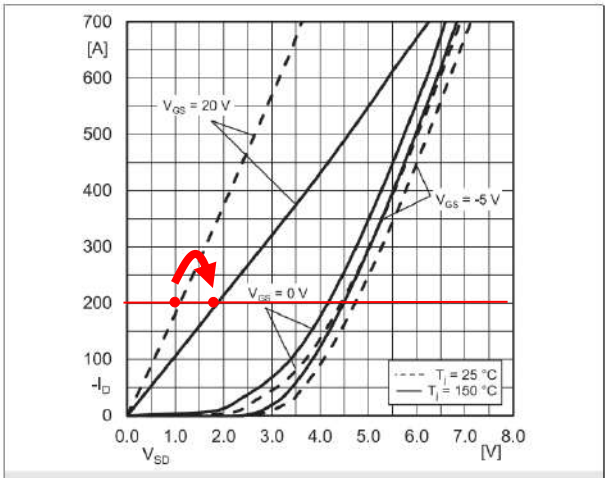
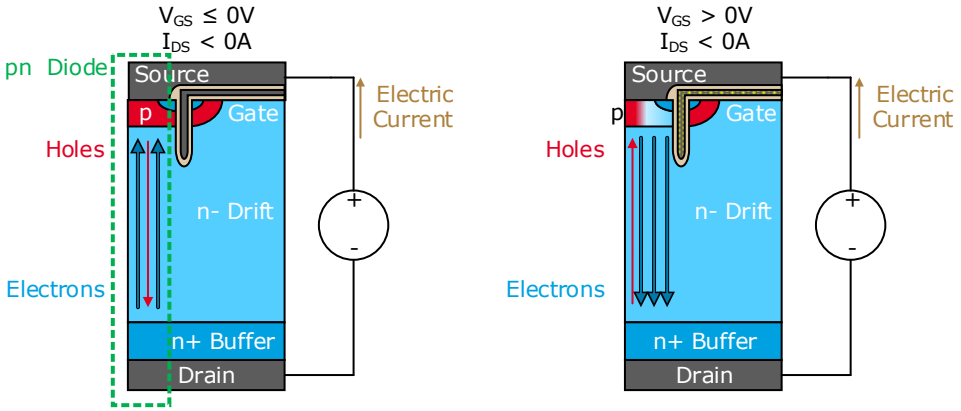


Fig. 2: Typ. reverse output characteristic, incl. $R_{DD'+SS'}$

The p-doped body and n-doped drift regions of a MOSFET form a pn diode. This "body" diode becomes forward biased (active) when the MOSFET is reverse biased.

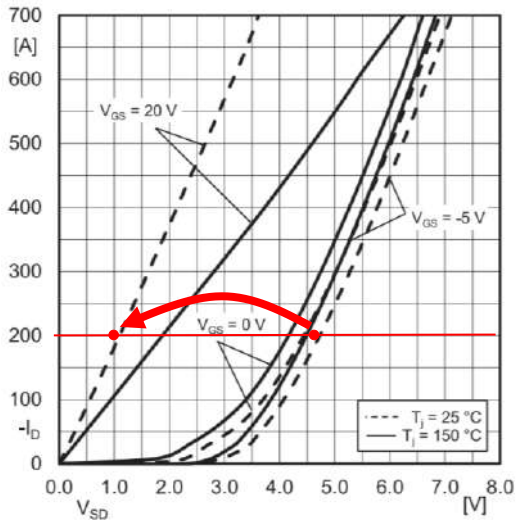
The body diode behaves like a typical pn diode, but with some added effects from the gate. As seen in Figure 4, the green box outlines the vertical slice within the MOSFET that is essentially a pn diode. With a negative gate voltage, only the diode is active. With reverse current, holes are generated and current flows. The current increases exponentially with the forward voltage drop.

Figure 4: Reverse conduction through body diode only (L) and body diode plus channel (R)



As the gate voltage is above 0V, the channel begins to open resulting in a lower impedance path for current to flow. If the gate is fully turned-on during reverse conduction, the forward voltage drop is greatly reduced (Figure 5).

Figure 5: Influence of gate voltage on reverse conduction (SKM350MB120SCH15)



2.2 Blocking state

Silicon carbide has a substantially higher breakdown electric field strength (V/cm) than silicon. This can be used to enable higher blocking voltages devices or to have thinner devices with the same blocking rating but with lower losses. Today's SiC MOSFETs are relatively thick with a lot of margin with regards to the blocking capability but the development tendency is clearly to reduce the thickness for even lower $R_{DS(on)}$ values.

The leakage current of silicon devices (I_{CES}) doubles roughly every 11°C. This can lead to thermal runaway at high temperatures, such as the extreme junction temperatures that occur following a short circuit, even if the device survives the initial pulse.

The leakage current of SiC MOSFETs tends to be substantially lower, but also increases at a lower rate than silicon devices. This is a major feature of SiC that can enable even higher junction temperature limits to be achieved.

3. Dynamic Behavior

3.1 MOSFET turn-on

The drain current is directly connected to the gate-source voltage during turn-on. A fast charging of the gate can lead to very high di/dt of 30…50 kA/µs which is 5 to 10 times higher than known from IGBT.

The usage of the integrated body diode as a commutation partner leads to recovery losses also in the MOSFET. A SiC SBD, on the other hand, produces nearly no reverse recovery current (I_{rr}). When used together with a MOSFET, the MOSFET turn-on current is greatly reduced, and therefore the turn-on losses (E_{on}) are also reduced. See [3] for more details on this topic.

3.2 MOSFET turn-off

The MOSFET turn-off losses (E_{off}) are quite low when compared to an IGBT. This is because MOSFETs are unipolar devices, meaning only electrons are used to carry current. In IGBTs, electrons and holes carry current, reducing the on-state voltage. However, during turn-off, the electron-hole pairs and resulting tail current cause substantially higher turn-off losses. Without the electron-hole plasma, MOSFETs can turn off faster and with lower losses. The di/dt and dv/dt of drain current and drain-source voltage can be well controlled by the gate, in contrast to an IGBT.

3.3 Body diode turn-off

Many SiC suppliers have put significant effort into improving the body diode's performance even when used without an SBD. This enables MOSFET-only products to be developed that have a considerable reduction in losses when compared to an IGBT-pn diode combination without the extra cost of a SiC chip or chips.

3.4 Short circuit behavior

During short circuit, hundreds of kilowatts or even megawatts of power can be dissipated into the chip. As a result, the junction temperature can reach hundreds of degrees. The amount of heating during short circuit is a function of the DC link voltage, short circuit current, duration of the pulse, and the thermal mass of the chip, among other factors.

The power dissipation during short circuit is produced almost entirely within the channel structure and only heats the surface of the chip, not the complete volume like in an IGBT. Higher gate voltages are often used to achieve the lowest possible $R_{DS(on)}$ with the drawback of even higher short circuit currents. Finally, SiC MOSFET chips are much smaller than an equivalent IGBT with a higher current density. Therefore, SiC MOSFETs reach critical temperatures at shorter pulses. Some SiC MOSFETs only allow short circuit durations of up to 2µs, while others are not capable of withstanding any short circuit.

3.5 Reverse bias safe operating area (RBSOA)

SiC MOSFETs can have a higher voltage overshoot during RBSOA than a similar IGBT. SiC MOSFETs tend to have a much higher switching speed resulting in a higher di/dt and dv/dt. This can cause oscillations during turn-off, leading to voltage spikes potentially exceeding the rating of the device.

When using SiC devices, great care must be taken to minimize the stray inductance of the commutation loop and maintain symmetry across the devices. This will help reduce the voltage overshoot and maintain current sharing. For this reason, new development is trending towards lower profile packages. For example, the SEMITRANS 3 package has been widely used, but new SiC products tend to be shorter, more compact modules, often with several parallel main terminals, such as the SEMITOP line.

3.6 Temperature dependency

Switching losses at 125°C and 150°C are quite close in value (Figure 6). However, switching losses have a slightly negative temperature coefficient. This is because the negative temperature coefficient of the threshold voltage means a higher gate current at higher temperatures. This is a drawback in paralleling in high switching frequency applications where switching losses dominate because a hot chip will take over even more current and have even higher losses.

To ensure good dynamic sharing, great care must be taken so that paralleled modules are as symmetrical as possible. The higher switching speeds of SiC MOSFETs relative to Si IGBTs means that this need is even greater. See [4] for more recommendations when paralleling modules.

Figure 6: SK250MB120CR03TE2

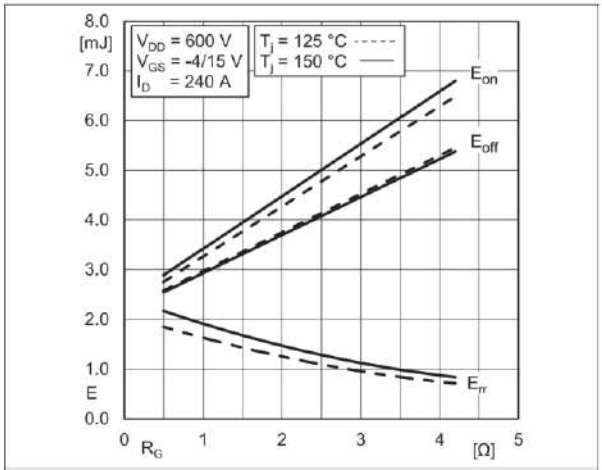


Fig. 5: Typ. turn-on /-off energy E = f (R_G)

4. Gate Drivers

4.1 Gate voltage

The allowable turn-on and turn-off voltages for SiC MOSFETs vary with chip technology (e.g. planar vs. trench gate) as there are generation-specific phenomena that must be avoided. The voltage selection then depends on a number of competing factors.

Turn-on voltage, $V_{GS(on)}$, must be:

- Maximized (more positive) for low conduction losses (low $R_{DS(on)}$)
- Minimized (closer to 0V) for high short-circuit capability (longer t_{psc})
- Minimized to avoid long term gate threshold voltage ($V_{GS(th)}$) drift

Turn-off voltage, $V_{GS(off)}$, must be:

- Maximized (more negative) to avoid parasitic turn-on of a switch in an off-state
- Minimized (closer to 0V) to avoid long term gate threshold voltage ($V_{GS(th)}$) drift

The recommended V_{GS} values given in the Characteristics section (7.2) of the module datasheet are specific to the used chip technology and have been selected to avoid any of the shortfalls listed above in typical applications.

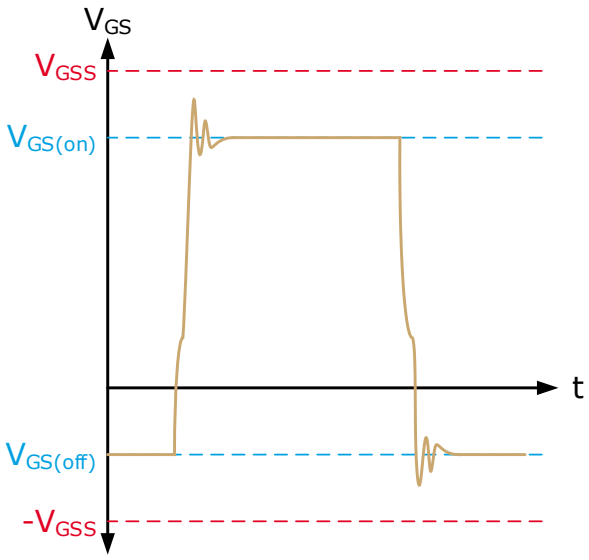
Figure 7: Location of recommended gate turn-on and turn-off voltages in Characteristics section of Semikron Danfoss datasheet (e.g. SK250MB120CR03TE2)

$t_{d(on)}$	V_{DD} = 600 V I_D = 240 A V_{GS} = -4/+15 V $R_{G\ on/off}$ = 0.5 Ω di/dt_{off} = 15 kA/µs di/dt_{on} = 22 kA/µs dv/dt = 29 kV/µs L_s = 5 nH	T_j = 150 °C	49	ns
$t_{d(off)}$		T_j = 150 °C	120	ns
t_r		T_j = 150 °C	17	ns
t_f		T_j = 150 °C	29	ns
E_{on}		T_j = 150 °C	2.97	mJ
E_{off}		T_j = 150 °C	2.57	mJ

The fast switching times of SiC devices, coupled with the parasitic inductance in the driver circuit, and/or displacement current across the semiconductor capacitances, can cause voltage overshoot during transitions as shown in Figure 8. In order to avoid exceeding the maximum gate voltage, it is recommended that the gate driver voltage supplies be designed such that there is no tolerance in one direction. For example, if the target turn-on/turn-off voltages, $V_{GS(on)}$/ $V_{GS(off)}$, for the device are +15V/-4V, then the gate driver power supplies should be regulated as follows:

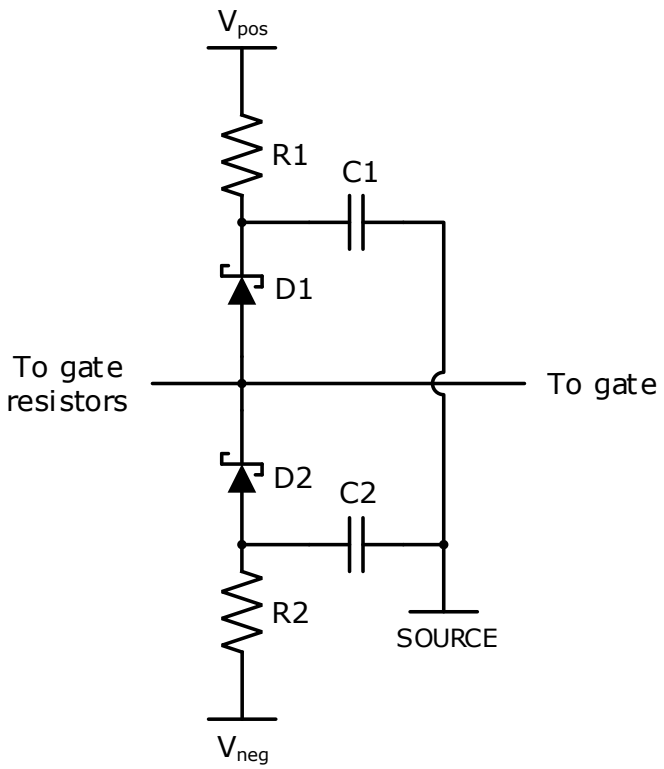
- V_{pos} = 15 +0/-1V
- V_{neg} = -4 -0/+1V

Figure 8: Definitions of turn-on and turn-off voltages with maximum values



A gate clamping circuit can also assist in avoiding gate overvoltage. The circuit shown in Figure 9 should be placed close to the module gate connection, with diodes D1 and D2 providing a return path to the negative and positive voltage rails for transient voltage spikes.

Figure 9: Example gate clamping circuit



R1, R2: 10Ω/0.1W
D1, D2: 60V/1A Schottky (e.g. SS16)
C1, C2: 1µF/50V

4.1.1 Measurement

V_{GS} is measured at the auxiliary (if equipped) module terminals to avoid the influence of any gate-source impedance between the driver and module. As the switching transitions for SiC applications are higher than with Si-based devices, a high-quality differential voltage probe is necessary to capture high frequency behavior (e.g. ringing).

Recommended probe characteristics:

- Bandwidth (-3dB): ≥100MHz
- Rise time: ≤3.5ns
- Lead length between measurement point and differential probe: <600mm, twisted where possible to reduce loop area.

4.2 Gate resistors

The effect of gate resistors on SiC MOSFETs is similar to that of Si devices in that lower gate resistance typically gives faster switching speeds and lower switching losses. Figure 10 gives a comparison between the switching losses vs. gate resistance for a fast 1200V Si IGBT and a 1200V SiC MOSFET.

Figure 10: Switching losses versus gate resistor for 120A/1200V Si (L) and 250A/1200V SiC (R) devices

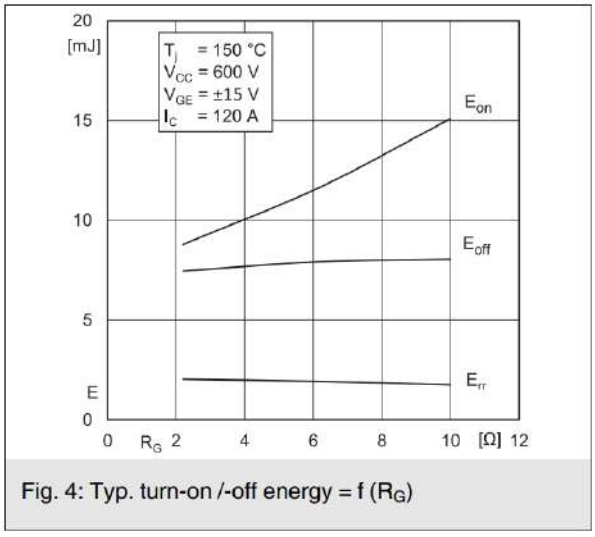


Fig. 4: Typ. turn-on /-off energy = f (R_G)

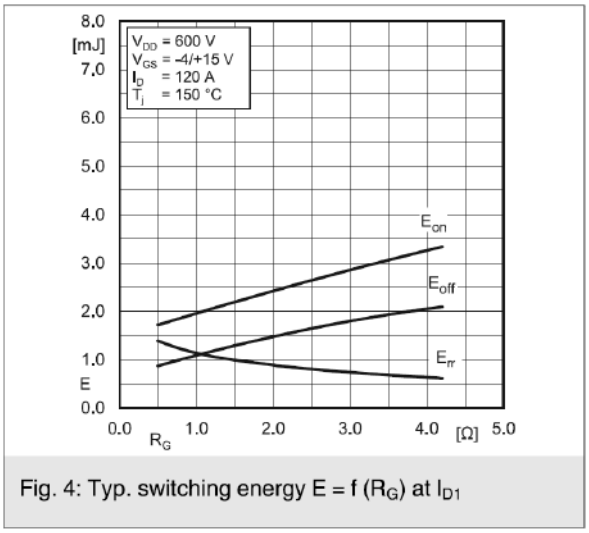


Fig. 4: Typ. switching energy E = f (R_G) at I_{D1}

SK120GB12F4T SK250MB120CR03TE2

As the rate of change of drain-source voltage, dv/dt, in a SiC MOSFET is inherently high (e.g. 50kV/µs), many users will use large gate resistors to reduce dv/dt.

For Semikron Danfoss IGBT modules, it has been stated [2] that twice the nominal current can safely be switched using the datasheet gate resistor. For SiC MOSFETs, this rule is not valid because the required gate resistor would be far too large. The current at which the losses are specified is only about 50% of the nominal current, because this is closer to operating conditions for applications with higher frequencies.

For more information on gate resistor selection, please refer to [5].

4.3 Gate inductance

The high-speed switching transitions of SiC devices means that minimizing gate inductance is crucial. Otherwise, large gate resistors are required to damp oscillations. A minimum gate resistance for damping oscillations can be calculated by:

$$R_{G,min} \geq \sqrt{\frac{L_G}{C_{iss}}}$$

Gate inductance can be reduced by reducing the loop area of the gate-source path between gate driver circuit and device. This is best achieved with a PCB-based design. The source node should be laid out on one layer as a larger plane. The gate signal is then placed on top of the layer immediately above the source.

4.4 Switching frequency

SiC has enabled higher switching frequencies for industrial power converters operating above 10kW. While this allows for reduced filtering, there are optimum design points for magnetics (in terms of cost/size/efficiency) that make switching at higher frequencies unnecessary. Also, the inherent issues with electromagnetic interference in high power converters are compounded by higher switching speeds as dv/dt and di/dt increase. Table 1 documents the maximum switching frequencies that have been observed in industry using presently available technology.

Table 1: Practical limits for hard switched converters (e.g. 100kW)		
Voltage Class	Si IGBTs	SiC MOSFETs
1200V	10...20kHz	30...60kHz
1700V	6...10kHz	20...40kHz

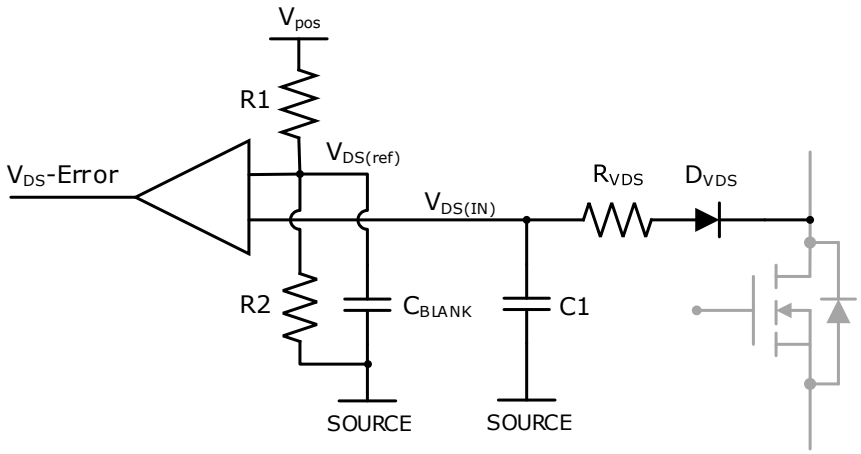
Increased switching frequency also impacts gate driver power requirements. The required power to be supplied by a given gate driver channel for a given power semiconductor device is directly proportional to the switching frequency (section 3.3 in [5]). Therefore, driver circuits that were suitable for a slower switching silicon-based design may not easily be adapted to SiC devices.

4.5 Short circuit detection

As noted in [Section 3], many generations of SiC MOSFETs have no, or very little, short circuit withstand capability. Additionally, the use of higher (>15V) gate voltages to reduce on-state losses also yields very high currents in the event of a short circuit (e.g. $>10 \cdot I_{Dnom}$). It is therefore critical that any short circuit detection circuitry act as fast as possible to give the best possible chance of device survival.

Short circuit detection for a SiC MOSFET is performed via monitoring of the on-state voltage drop across the device in a manner similar to that used with a Si IGBT (i.e. DESAT, DSCP). A comparator circuit is used where the on-state voltage is measured via a blocking diode, as shown in Figure 11. The blanking time can be set to a few 100ns, which is possible because V_{DS} drops very quickly. For example, switching 600V with 10kV/µs means a V_{DS} drops to its minimum value within 60ns.

Figure 11: Example DESAT detection circuit



D_{VDS}: Blocking diode, fast recovery, high voltage (e.g. BY203-20S)
R_{VDS}: Voltage dropping resistor (application dependent)
C1: Filter capacitor, for noise suppression, as low a value as possible (e.g. <1nF)
R1/R2: Voltage divider to set static trip voltage (application dependent)
C_{BLANK}: Capacitor to set blanking time (application dependent)

4.6 Parasitic turn-on

As described in [11], for silicon devices parasitic turn-on can be caused by the feedback effect of the Miller capacitance or by the influence of the parasitic inductance in the emitter (source) branch.

SiC MOSFETs have a lower gate threshold voltage than Si IGBTs (e.g. $V_{GS(th)} \approx 2.5V$ vs. $V_{GE(th)} \approx 5.8V$). This characteristic, coupled with the higher dv/dt and di/dt inherent in high-speed switching and the gate capacitance ratios typical of SiC MOSFETs, means that SiC MOSFET devices are at a higher risk for parasitic turn-on than Si devices.

The gate clamping circuit shown in Figure 9 also provides some protection against parasitic turn-on.

The susceptibility of a SiC MOSFET to parasitic turn-on is dictated by the ratio of gate capacitances. At high dv/dt, the impressed voltage across the gate can be estimated using the following equation:

$$\Delta V_{GS} = \Delta V_{DG} \cdot \frac{C_{rss}}{C_{iss} - C_{rss}}$$

...where $\Delta V_{DG} \approx V_{DC}$ in the case of a half-bridge circuit.

If the impressed voltage is greater than the turn-off voltage plus the threshold voltage, the device will likely be inadvertently turned on.

Example:
A SiC MOSFET is switched with a $600V_{DC}$ link and uses $V_{GS(off)}$ = -4V. The datasheet for the SiC MOSFET gives C_{rss} = 27pF, C_{iss} = 1337pF, and $V_{GS(th)}$ = 4.15V. The impressed voltage during switching is:

$$\Delta V_{GS} = 600V \cdot \frac{27pF}{1337pF - 27pF} = 12.37V$$

The gate voltage could potentially reach:

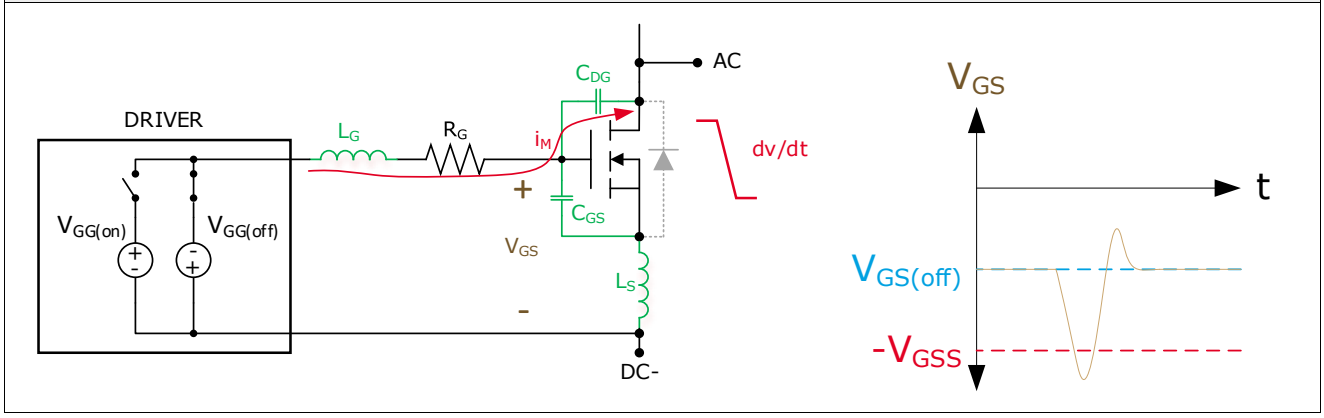
$$V_{GS(pk)} = -4V + 12.7V = 8.37V$$

This value is above the threshold voltage of 4.15V, which means the device could be turned on.

4.6.1 Excessive negative gate voltage

Parasitic turn-on via Miller capacitance current is caused by large values of positive dv_{DS}/dt. Large values of dv_{DS}/dt in the negative direction can induce negative gate voltage. Since SiC MOSFETs can only tolerate a relatively small negative gate voltage, any induced voltage spikes could cause damage to the device. In Figure 12, a fast-falling voltage from AC to DC- (across drain to source), induces a current flow from gate to source via the Miller capacitance. This current generates a negative voltage drop across the impedances in the gate circuit. This voltage drop adds to the negative turn-off gate voltage supplied by the driver.

Figure 12: Miller current-induced negative gate voltage overshoot



Both parasitic turn-on and excessive negative gate voltage can be avoided using a Miller clamp circuit. A MOSFET is connected between gate and source of the power device on the gate driver. When the power device is in the off-state, the gate driver circuit keeps this MOSFET on. The MOSFET effectively short-circuits the Miller current, preventing it from creating a voltage drop across the impedances in the gate circuit (e.g. L_G, R_G). Modern gate driver ICs incorporate such a MOSFET internally, meaning only an additional gate connection is required.

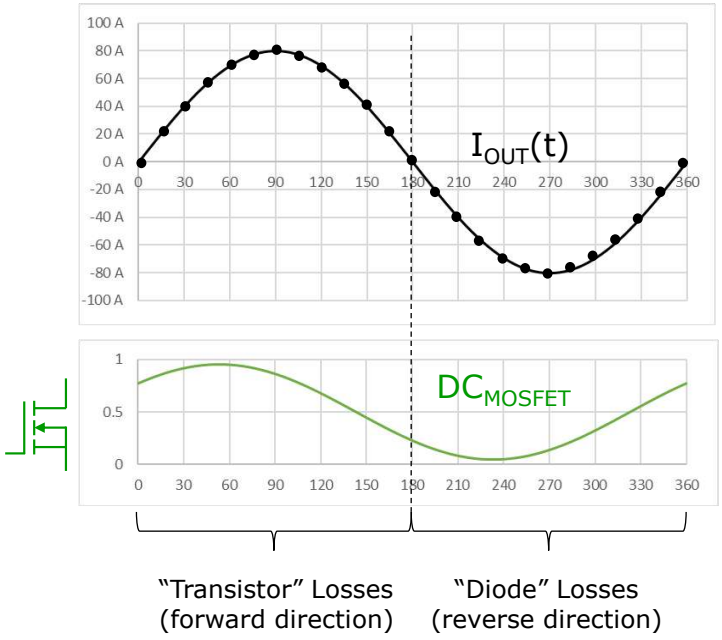
5. Losses

Losses in a SiC MOSFET are considered in a similar manner to Si IGBTs, wherein the total losses are divided into conduction and switching losses. However, an additional feature in a MOSFET (compared to IGBTs) is the

ability to use the channel in reverse conduction for negative (source-to-drain) currents (see section 2.1). In most voltage source inverter topologies (as well as synchronous rectifiers in DC/DC topologies), the PWM generated by the controller already alternates switching between the upper and lower switches in a half-bridge, meaning the channel of the MOSFET is already available for conduction of reverse currents. This means that reverse currents can flow in the MOSFET channel, body diode, and external SBD (if equipped).

The following formulae are given in a general time-based manner to show the general approach to loss calculation. These formulae can be extended to a point-by-point calculation method using spreadsheet software, though the temperature-dependent effects (which require recursion) and module parameter database are best handled with a dedicated thermal calculation tool.

Figure 13: Generic example of sampled current and corresponding MOSFET duty cycle



5.1 MOSFET only (no external diode)

5.1.1 Conduction losses

During forward conduction, as the MOSFET does not have an intrinsic forward voltage drop resulting from a pn junction, conduction losses in the channel are calculated only considering the on-state resistance. A generic duty cycle is shown, which must be calculated based on the circuit topology, switching pattern, and operating conditions.

$$V_{DS}(t) = I_{OUT}(t) \cdot Ki_{MOSFET}(t) \cdot R_{DS(on)}\left(T_j(t)\right)$$

$$P_{cond(MOSFET)}(t) = I_{OUT}(t) \cdot Ki_{MOSFET}(t) \cdot V_{DS}(t) \cdot DC_T(t)$$

During reverse conduction, the current is divided between the MOS channel and the body diode. It is easiest to determine the current sharing using a circuit simulator or with an iterative set of equations (e.g. in spreadsheet software). Therefore, for the purpose of this discussion a current sharing factor, Ki, is used to indicate that a portion of the total current is flowing through each device.

$$Ki_{MOSFET}(t) + Ki_{body\ diode}(t) = 1$$

In forward conduction, Ki_{MOSFET} = 1 and $Ki_{body\ diode}$ = 0. In reverse conduction, the Ki_{MOSFET} and $Ki_{body\ diode}$ will each be less than one depending on the current sharing between the MOS channel and the body diode.

Conduction losses in the MOS channel are calculated above but since the body diode has a pn junction, the conduction losses are calculated in the traditional manner with the straight-line approximation of the forward characteristic.

$$V_f(t) = V_{F0}\big(T_j(t), t\big) + I_{OUT}(t) \cdot Ki_{body\ diode}(t) \cdot r_f\big(T_j(t)\big)$$

$$P_{cond(body\ diode)}(t) = I_{OUT}(t) \cdot Ki_{body\ diode} \cdot V_f(t) \cdot DC_D(t)$$

During dead time, the channels of both upper and lower MOSFETs in a half-bridge circuit are off, meaning any negative current will only flow through the body diode (i.e. Ki_{MOSFET} = 0, $Ki_{body\ diode}$ = 1).

5.1.2 Switching losses

Switching losses consist of the turn-on and turn-off losses of the MOSFET, as well as the reverse recovery behaviour of the intrinsic body diode:

$$P_{sw(MOSFET)}(t) = f_{sw} \cdot \big[E_{on}\big(V, I_{OUT}(t), T_j(t)\big) + E_{off}\big(V, I_{OUT}(t), T_j(t)\big)\big]$$

$$P_{sw(body\ diode)}(t) = f_{sw} \cdot \big[E_{rr}\big(V, I_{OUT}(t), T_j(t)\big)\big]$$

As explained further in [3], the value of E_{rr} for the diode contains: E_{rr} for the body diode, E_{pto} for the MOSFET, and E_{CJ} for the MOSFET. However, since these losses all occur in the same physical semiconductor, they are not calculated separately. In most cases, E_{CJ}, which does not contribute to the real losses, is neglected but in certain applications it must be subtracted from Err before calculating losses.

5.2 MOSFET + external SBD

5.2.1 Conduction losses

Modules employing an additional Schottky barrier diode (SBD) offer a third path for current during reverse conduction and thus a portion of the overall current is accounted for with another current sharing factor.

$$Ki_{MOSFET}(t) + Ki_{body\ diode}(t) + Ki_{SBD}(t) = 1$$

As an SBD has an intrinsic voltage drop, the conduction losses are again calculated in the traditional manner with the straight-line approximation of the forward characteristic.

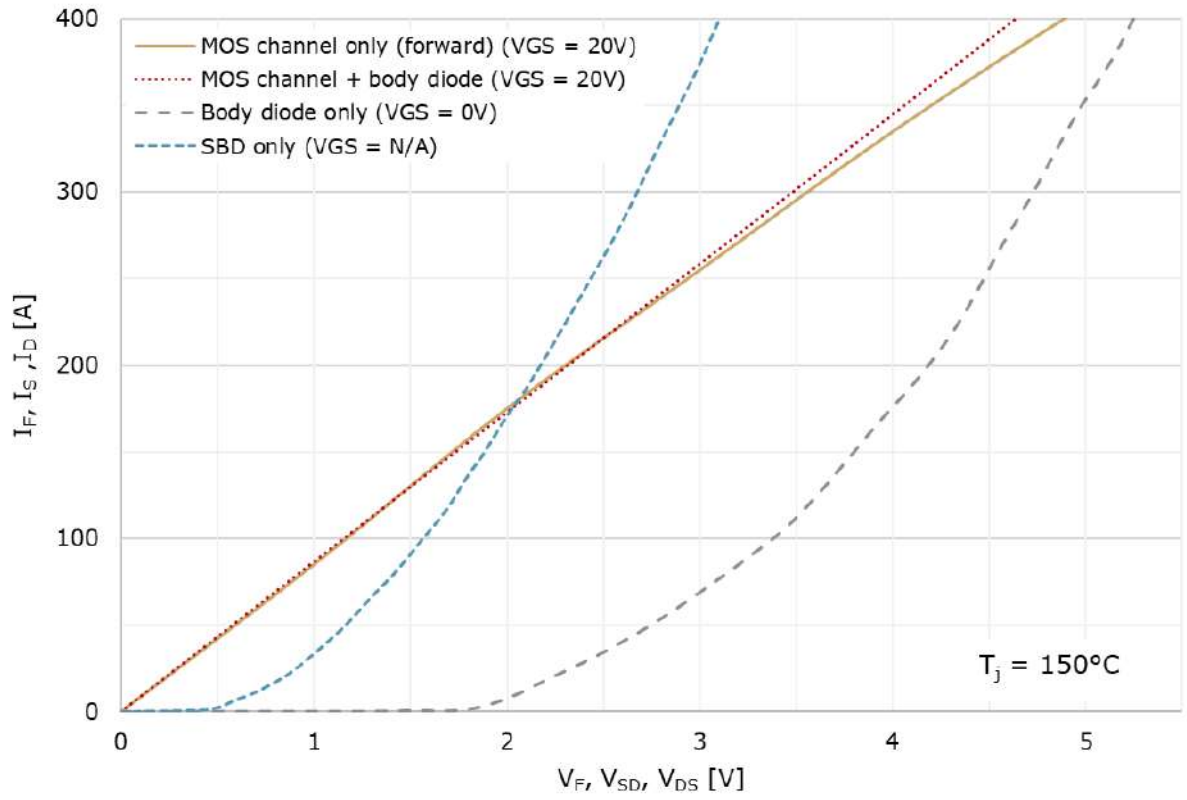
$$V_f(t) = V_{F0}\big(T_{j,SBD}(t), t\big) + I_{OUT}(t) \cdot Ki_{SBD}(t) \cdot r_f\big(T_{j,SBD}(t)\big)$$

$$P_{cond(SBD)}(t) =\cdot I_{OUT}(t) \cdot Ki_{SBD}(t) \cdot V_f(t) \cdot DC_D(t)$$

During interlock time, Ki_{MOSFET} = 0 and Ki_{SBD} and $Ki_{body\ diode}$ represent the share of the current between the two diodes.

The relative voltage drops between the three different paths (MOS channel, body diode, and SBD) are shown in Figure 14.

Figure 14: Comparison of voltage drops in different devices (~160A devices)



5.2.2 Switching losses

Switching losses of a Schottky barrier diode are considered negligible (due to its unipolar nature) and are therefore not given in datasheets. Instead $E_{rr(MOSFET)}$ is given to indicate that the losses occur in the MOSFET chip (see [3] for explanation).

$$P_{sw(MOSFET)}(t) = f_{sw} \cdot \left[E_{on}\left(V, I_{OUT}(t), T_j(t)\right) + E_{off}\left(V, I_{OUT}(t), T_j(t)\right)\right]$$

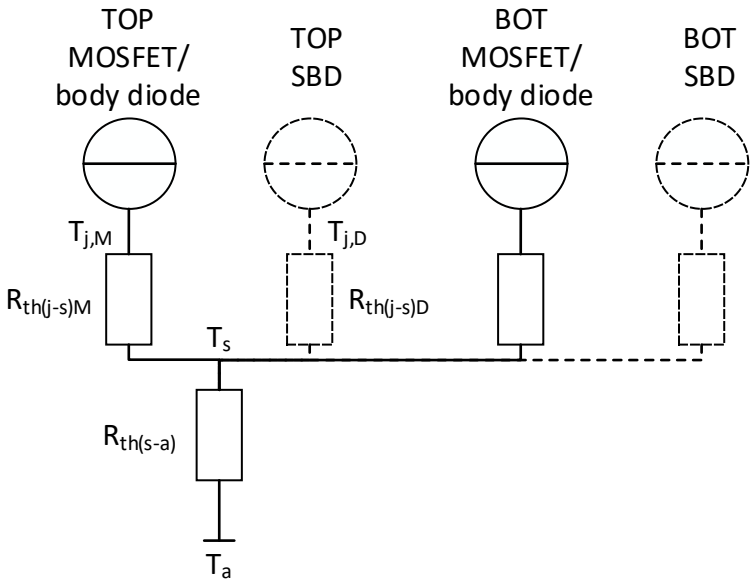
$$P_{sw(body\ diode)}(t) = f_{sw} \cdot \left[E_{rr(MOSFET)}\left(V, I_{OUT}(t), T_j(t)\right)\right]$$

$$P_{sw(APD)}(t) \approx 0$$

5.3 Junction temperature calculation

With losses calculated, temperature calculation is performed in a similar manner as with Si devices, using the Foster thermal equivalent circuit diagram [2]. As the body diode is part of the MOSFET chip, the losses are generated in the same physical space. Thus, the junction temperature of the body diode and MOS channel are the same, and both devices use the same value of thermal resistance. The anti-parallel Schottky body diode, if equipped, has its own junction temperature and thermal resistance (see Figure 15). For a more detailed description of how these thermal resistances are defined, including for baseplate modules, see [10].

Figure 15: Thermal equivalent circuit diagram for a baseplate-less half-bridge SiC MOSFET module (w/ and w/o anti-parallel diodes)



6. Reliability

6.1 Gate oxide

SiC gate oxide can be more sensitive than similar silicon structures. As discussed above, this can mean stricter limits on the gate voltage maximum values. However, this sensitivity also introduces some other concerns regarding long term reliability. The gate voltage must be kept within the datasheet limits, otherwise long-term shifts or damage could occur.

Gate cables and PCB traces should be kept to a minimum using twisted pairs and overlapping ground layers when possible. This will minimize the gate inductance and therefore over and undershoots in gate voltage. This will help ensure that the threshold of the device does not shift over time. If V_{Gth} drifts upwards, the R_{DSon} of the chip will also increase, raising the conduction losses. Dynamic behaviour can also be altered.

6.2 Power cycling

Silicon carbide is a considerably stiffer material than silicon, having a roughly three times higher Young's Modulus. SiC devices tend to come in smaller sizes compared to a similarly rated IGBT chip. This smaller geometry results in a higher strain in the corners of the device.

SiC devices often have substantially lower losses than equivalent silicon devices and can enable a lower temperature swing for the same load profile.

SiC and Si should not be directly compared in terms of power cycling lifetime. These aspects must be balanced when designing a new system. [6] provides the basis for performing such calculations.

6.3 Humidity

The construction of SiC chips is not radically different from Si devices so the failure modes are similar, and the same precautions must be taken (see [9]). In general, the latest SiC chipsets are capable of passing the HV-H³TRB test (per EN 60749-5:2018) to 1000 hours. As the chip voltage rating, module design, and module production process also have an impact on humidity robustness, the actual test duration for a specific module family may vary.

6.4 Cosmic radiation

Cosmic ray failures occur when a high energy particle interacts with a semiconductor while blocking. This causes a local disturbance of the electric field inside the chip, potentially leading to a local breakdown and failure.

Although both Si and SiC chips are susceptible to this failure mode, SiC chips have an advantage over Si. SiC chips tend to be much smaller than their Si equivalents. A smaller area gives a lower probability that a particle will pass through the chip, and therefore a lower rate of cosmic ray failure rate.

[7] serves as the basis for calculating failures rates due to cosmic radiation.

6.5 Body diode

Some older generation SiC MOSFETs showed some degradation and shifts over time if the body diode was used. However, the modern designs used by Semikron Danfoss do not have this drawback. The body diodes of the SiC MOSFETs in Semikron Danfoss modules are safe to use in forward operation within the limits defined in their respective datasheets.

7. Datasheets

The characteristics of new SiC MOSFET modules require some changes to the terminology traditionally used in silicon MOSFET datasheets [2]. The following terms are used in datasheets for SiC MOSFET devices for product from 2023 onward.

In the datasheets, the values are specified separately for each module component (or module function, such as forward and negative conduction behaviour of MOSFET). All ratings refer to one switch, irrespective of the number of MOSFET chips per switch actually connected in parallel in the transistor module.

Only terms specific to SiC MOSFET datasheets or different from Si IGBT datasheets are explained below. For an explanation of terms related to the Schottky barrier diode (SBD) often used in anti-parallel with a MOSFET, please refer to AN 22-001 [3].

7.1 Absolute maximum ratings, MOSFET and integrated body diode

These values are given in the first section of the datasheet (Figure 16) and should be considered design limits that cannot be exceeded during operation.

Figure 16: Absolute maximum ratings, MOSFET and integrated body diode

Absolute Maximum Ratings				
Symbol	**Conditions**		**Values**	**Unit**
MOSFET				
V_{DSS}	T_j = 25 °C		1200	V
I_D	HPTP / HP-PCM T_j = 175 °C	T_s = 70 °C	29	A
		T_s = 100 °C	25	A
I_{DM}	PW ≤ 10µs, Duty cycle ≤ 1%		84	A
V_{GS}	Transient Gate - Source voltage (t<300ns)		-4 ... +23	V
T_j			-40 ... 175	°C
Integrated body diode				
I_{SM}	PW ≤ 500ns, Duty cycle ≤ 5%		43	A
I_{FSM}	PW ≤ 10µs		84	A

7.1.1 MOSFET: continuous drain current, I_D

Calculated maximum direct current at the drain at which the permissible chip temperature is reached. The current is calculated with a fixed case or heatsink temperature and $T_j = T_{j(max)}$

$$I_D = \sqrt{\frac{T_j - T_n}{R_{th(j-n),max} \cdot R_{DS(on),max,Tj}}}$$

…where n is sink or case, depending on whether the module has a baseplate.

Since I_D designates a static value (direct current), it is not relevant for switching operation. The value is used only as a comparison to other devices to give an indication of the current capability.

7.1.2 MOSFET: peak value of pulsed drain current, I_{DM}

Repetitive peak drain current that the MOSFET (in on-state) is able to withstand under normal operation without damage. The duration of the current pulse must be limited to prevent the junction temperature from exceeding $T_{j(max)}$.

This value is similar to I_{CRM} for a Si IGBT and is valid for current flowing in either direction through the on-state drain-source channel.

7.1.3 MOSFET: gate-source voltage, V_{GSS}

Maximum voltage (indicated as transient or static) between the gate and source terminals with drain-source shorted ($V_{DS} = 0$).

This value varies with chip technology (i.e. chip generation). Recommended gate-source drive voltages are given in the Characteristics section of the datasheet (7.2).

7.1.4 MOSFET: maximum turn-on time during short-circuit, t_{psc}

Maximum duration of desaturation caused by overcurrent or short-circuit at a specified supply voltage, drain-source voltage, and junction temperature.

The short-circuit protection circuitry (e.g. DSCP, DESAT detection) must interrupt the current within t_{psc} in order to avoid device destruction. This value varies with chip technology (i.e. chip generation). If no value is present, the chip does not have any guaranteed short circuit capability.

7.1.5 Integrated body diode: peak value of pulsed forward current, I_{SM}

Repetitive peak forward current that the body diode (MOSFET in off-state) is able to withstand under normal operation without damage. The duration of the current pulse must be limited to prevent the junction temperature from exceeding $T_{j(max)}$.

This value is similar to I_{FRM} for a Si FWD.

7.1.6 Integrated body diode: surge forward current, I_{FSM}

Non-repetitive peak forward current in the form of a half-sine wave with pulse width, t_p, that the body diode (MOSFET in off-state) is able to withstand in the event of a malfunction (e.g. short-circuit), provided it does not occur too often during the diode lifetime.

When the device is subjected to a current near I_{FSM}, the junction temperature can reach values in excess of $T_{j(max)}$, causing damage to the chip metallization. Additionally, the blocking voltage capability of the diode immediately following the surge current event is reduced. The datasheet value of I_{FSM} is valid for an event in which the diode is not expected to block any reverse voltage.

7.2 Characteristics

These values are given in the second section (Figure 17) of the datasheet and define the behavior of the device under recommended operating conditions.

Figure 17: Characteristics, MOSFET and integrated body diode

Characteristics					
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
MOSFET						
$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 9.2 mA, T_j = 25 °C		1200			V
$V_{GS(th)}$	V_{DS} = 10V, I_D = 11.1 mA, T_j = 25 °C		2.8		4.8	V
I_{DSS}	V_{GS} = 0 V, V_{DS} = 1200 V, T_j = 25 °C				0.2	mA
I_{GSS}	V_{DS} = 0 V, V_{GS} = 21 V, T_j = 25 °C				400	nA
$R_{DS(on)}$	V_{GS} = 18 V, I_D = 21 A, chiplevel	T_j = 25 °C		36	45	mΩ
		T_j = 150 °C		72		mΩ
C_{iss}	V_{GS} = 0 V, V_{DS} = 800 V, T_j = 25 °C	f = 1 MHz		2335		pF
C_{oss}		f = 1 MHz		70		pF
C_{rss}		f = 1 MHz		5		pF
Q_G	V_{GS} = 0…18V, V_{DS} = 800V, I_D = 21 A			91		nC
R_{Gint}	T_j = 25 °C			1.0		Ω
$t_{d(on)}$	V_{DD} = 600 V I_D = 30A V_{GS} = 0/18 V R_{Gon} = 3.3 Ω R_{Goff} = 3.3 Ω di/dt_{on} = 2.9 kA/µs di/dt_{off} = 1.7 kA/µs dv/dt_{on} = 29 kV/µs dv/dt_{off} = 29 kV/µs Lσ = 14 nH	T_j = 150 °C		10		ns
t_r		T_j = 150 °C		9		ns
$t_{d(off)}$		T_j = 150 °C		52		ns
t_f		T_j = 150 °C		30		ns
E_{on}		T_j = 150 °C		0.32		mJ
E_{off}		T_j = 150 °C		0.26		mJ
t_{psc} [1]	V_{DD} ≤ 720 V V_{DSS} < 1200 V V_{GS} = 0/18 V E_{sc} ≤ 280 mJ	T_j = 150 °C	2			µs
$R_{th(j-s)}$	per MOSFET, HPTP / HP-PCM			1.25		K/W
Integrated body diode						
$V_F = V_{SD}$	$-I_D$ = 21 A V_{GS} = 0 V chiplevel	T_j = 25 °C		3.30		V
		T_j = 150 °C		3.60		V
$V_{F0} = V_{SD0}$	chiplevel	T_j = 25 °C		2.25		V
		T_j = 150 °C		2.10		V
$r_F = r_{SD}$	chiplevel	T_j = 25 °C		50		mΩ
		T_j = 150 °C		71		mΩ
t_{rr}	V_{DD} = 600 V I_D = 30 A V_{GS} = 0 V di/dt_{off} = 2.8 kA/µs	T_j = 150 °C		54		ns
Q_{rr}		T_j = 150 °C		1		µC
I_{rr}		T_j = 150 °C		37		A
E_{rr}		T_j = 150 °C		0.39		mJ

7.2.1 MOSFET: drain-source breakdown voltage, $V_{(BR)DSS}$

Breakdown voltage between drain and source with gate-source shorted (V_{GS} = 0V). Value given for impressed current, I_D, and junction temperature, T_j.

$V_{(BR)DSS}$ is measured with a high-voltage constant-current source so the stated current (I_D) does not necessarily correspond to the leakage current (I_{DSS}). As most SiC MOSFET devices do not explicitly allow operation in the avalanche region, $V_{(BR)DSS,min}$ will usually be equal to V_{DSS}.

7.2.2 MOSFET: Gate-source leakage current, I_{GSS}

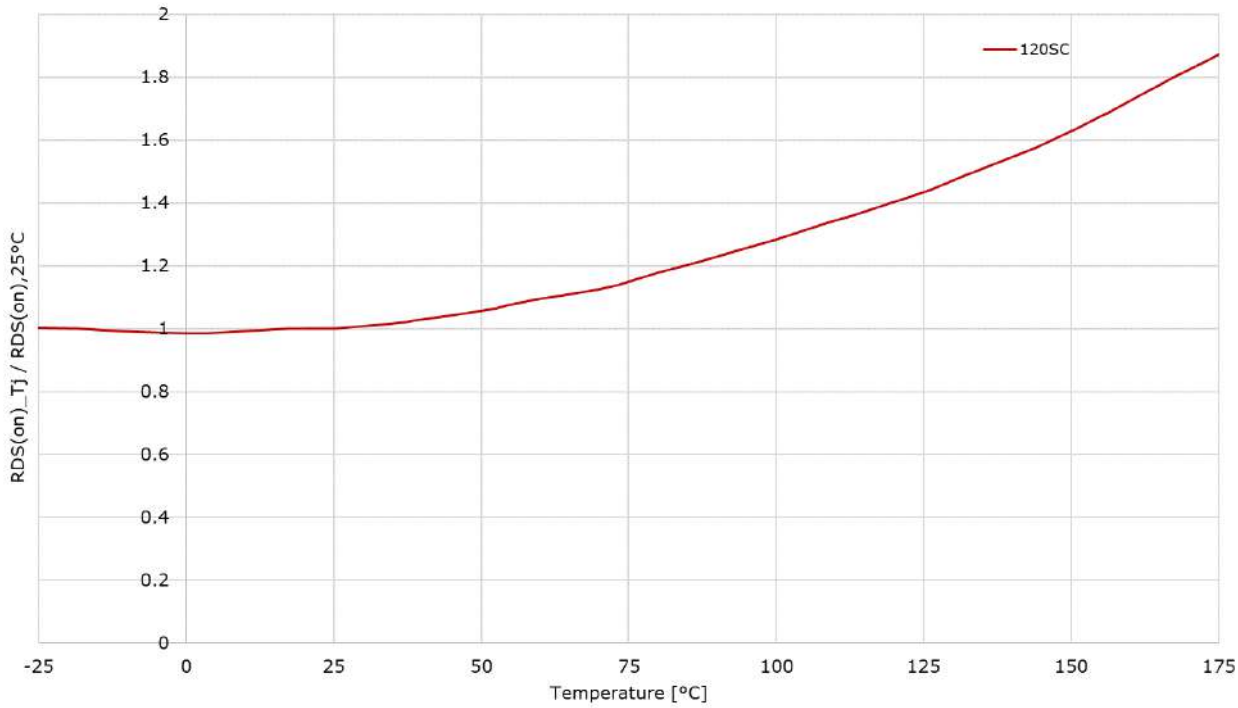
Leakage current between gate and source with drain-source shorted (V_{DS} = 0) at specified drain-source voltage, temperature, and gate voltage.

7.2.3 MOSFET: Drain-source turn-on resistance, $R_{DS(on)}$

Quotient of changing drain-source voltage, V_{DS}, and drain current, I_D, in a fully gate-controlled MOSFET at a specified gate-source voltage, drain current (i.e. "rated current"), and junction temperature.

$R_{DS(on)}$ is strongly dependent on $V_{GS(on)}$ and T_j (see section 2.1 and Figure 18).

Figure 18: $R_{DS(on)}$ vs. temperature, normalized to 25°C



7.2.4 Body diode: reverse recovery energy, E_{rr}

Reverse recovery energy of the body diode during turn-off as measured under the specified conditions.

7.2.5 Current class

Power MOSFET devices have traditionally been classified by their drain-source turn-on resistance. IGBT modules have been classified by the nominal current (DC) rating of the chips that make up each functional IGBT switch. Semikron Danfoss SiC MOSFET module names contain an approximate current class that is derived from the test current used for deriving the characteristics given in the datasheet. This test current, I_D or $-I_D$, is shown in the "Conditions" section for a given characteristic.

However, due to the low switching losses in SiC, this current rating is of little use when comparing to a silicon device (e.g. a 250A IGBT would often be replaced by a smaller SiC MOSFET).

Symbols and Terms

Letter Symbol	Term
SiC	Silicon Carbide
Si	Silicon
SBD	Schottky barrier diode
APD	Anti-parallel diode (freewheeling diode, inverse diode)

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors"

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